CLAIMS:

1. A method of forming a semiconductor device, comprising:

forming one or more sacrificial layers on at least a portion of the top surface of the semiconductor device;

annealing at least a portion of the semiconductor device; and

removing a substantial portion of the one or more sacrificial layers, wherein the removing results in no substantial physical alterations to the semiconductor device.

2. The method of claim 1, wherein said forming comprises one or more deposition processes.

3. The method of claim 1, wherein at least one of said one or more sacrificial layers comprises a phosphorous doped polysilicon layer.

4. The method of claim 1, wherein at least one of said one or more sacrificial layers comprises a metal nitride layer.

5. The method of claim 4, wherein said metal nitride comprises titanium nitride.

6. The method of claim 1, wherein the at least one sacrificial layer is formed to layer a substantial portion of the top surface of the semiconductor device.

7. The method of claim 1, wherein said annealing comprises a laser annealing.

8. The method of claim 1, wherein said annealing comprises a rapid thermal annealing (RTA).

9. The method of claim 1, wherein said removing comprises selective removing, wherein the selective removing comprises an etch that removes a substantial portion of the one or more sacrificial layers, selective to the top surface of the semiconductor device.

10. The method of claim 9, wherein selective removing comprises removing one or more sacrificial layers by using one or more chemicals selected based on the chemicals ability to remove one or more sacrificial layers without substantial removal of other materials on the semiconductor device.

11. The method of claim 1, wherein said removing comprises a wet-etch.

12. The method of claim 11, wherein said wet etch comprises a hydroxide based wet etch.

13. The method of claim 11, wherein said wet etch comprises a sulfuric acid/oxidant based wet etch.

14. The method of claim 1, wherein the semiconductor device comprises one or more transistors embodied on a silicon wafer.

15. A method of annealing a silicon wafer, comprising:

at least partially forming a transistor on a silicon wafer;

forming one or more sacrificial layers on at least a portion of the silicon wafer;

annealing at least a portion of the silicon wafer; and

removing a substantial portion of the one or more sacrificial layers.

16. The method of claim 15, further comprising removing a substantial portion of the one or more sacrificial layers without substantial removal of one or more other materials forming the silicon wafer.

17. The method of claim 15, wherein said forming one or more sacrificial layers comprises depositing one or more materials through one or more chemical vapor deposition processes.

18. The method of claim 15, wherein said forming one or more sacrificial layers comprises heating the silicon wafer while in the vicinity of one or more gaseous materials.

19. The method of claim 15, wherein at least a portion of the sacrificial layer is comprised of phosphorous doped polysilicon.

20. The method of claim 15, wherein at least a portion of the sacrificial layer comprises a metal nitride layer.

21. The method of claim 20, wherein said metal nitride comprises titanium nitride.

22. The method of claim 15, wherein said annealing comprises one or more laser annealing processes.

23. The method of claim 15, wherein said annealing comprises a rapid thermal annealing (RTA).

24. The method of claim 15, wherein said removing comprises a wet-etch.

25. The method of claim 24, wherein said wet etch comprises a hydroxide based wet etch.

26. The method of claim 24, wherein said wet etch comprises a sulfuric acid/oxidant based wet etch.

27. A semiconductor apparatus, comprising:

a substrate of silicon having one or more dopant impurities implanted in at least a portion of the substrate;

a gate dielectric layer formed on at least a portion of the substrate;

a conductive gate formed on the gate dielectric layer;

one or more spacers formed proximate to the conductive gate and gate dielectric layer;

an interlayer dielectric formed proximate to the substrate; and

one or more sacrificial layers formed adjacent to the interlayer dielectric.

28. The device of claim 27, wherein the apparatus comprises one or more integrated circuits (IC).

29. The device of claim 27, wherein one or more dopant impurities is implanted by ion implantation.

30. The device of claim 27, wherein the one or more sacrificial layers comprises phosphorous doped polysilicon.

31. The device of claim 27, wherein the one or more sacrificial layers comprise a metal nitride layer.

32. The device of claim 31, wherein the metal nitride comprises titanium nitride.

33. The device of claim 27, wherein the one or more sacrificial layers is formed by use of one or more chemical vapor deposition processes.

34. The method of claim 27, wherein said forming one or more sacrificial layers comprises heating the silicon wafer while in the vicinity of one or more gaseous materials.